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COMPENSATION DESIGN FOR SWITCHING POWER SUPPLY IN BUCK TOPOLOGY AND VOLTAGE MODE CONTROL

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ABSTRACT

The objective of this work is to design a compensation network for a buck converter in voltage mode control with efficiency higher than 70%, to convert the unregulated voltage of 20V to 40V into a well regulated output voltage of 5V, supplying an output current in the range of 2A to 10A. The output voltage ripple should be lower than 100mV peak-to-peak. This document also includes the complete DC/DC converter design along with a theory description, components evaluation and test results.

PROJETO DE UM COMPENSADOR PARA FONTE CHAVEADA NA TOPOLOGIA "BUCK" E MODO DE CONTROLE POR TENSÃO

RESUMO

O objetivo deste trabalho é o projeto de um compensador para um conversor tipo "buck" no modo de controle por tensão com eficiência maior que 70% tendo como entrada a tensão desregulada de 20V a 40V e saída, tensão regulada a 5V, corrente de saída entre 2A e 10A. O "ripple" na tensão de saída deve ser menor que 100mV pico a pico. Este documento também inclui o projeto completo do conversor DC/DC junto com a teoria, cálculos dos valores dos componentes e resultados de teste.

SUMARY

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1 - Introduction

Like any other switching power supply, the basic idea behind a buck converter is to control the output voltage by switching the input voltage by means of a pulse width modulation (PWM). Therefore the output voltage is an average of the input. Figures 1 and 2 bellow illustrates this process. Here the switch is closed and opened very rapidly during the time the system is working.

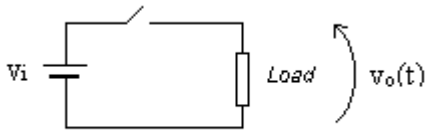

FIGURE 1- Regulation Concept.

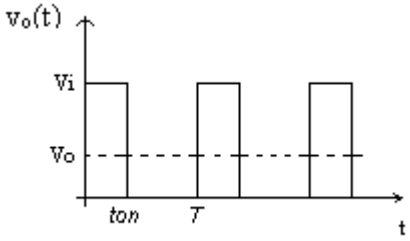

FIGURE 2 – Ideal waveform obtained by switching the input and corresponding d-c output voltage level.

In the figure above we use capital letters to represent dc quantities and small letters to time variant variables. So, the dc component V_o will be the average value of the function $v_o(t)$. Equation 1 gives this value, which can be easily calculated by evaluating the area under the curve.

$$V_o = \frac{1}{T}\int_0^T v_o(t)dt \tag{1}$$

$$V_o = V_i \frac{t_{on}}{T} \tag{2}$$

$$V_o = V_i d \tag{3}$$

f_s is the frequency applied to the switch and it's the inverse of the period T. Equation 3 shows another way of viewing the dc output voltage where the factor *d* is called duty cycle. A problem arises when we switch the input as we did because a waveform signal like the one in fig. 2 will contain harmonics that needs to be filtered out. This periodic signal may be expressed in the form of Fourier series, like the one shown in equation numbered (4). Note the first term as the dc component plus the harmonics whose lowest frequency is exactly the switching frequency. So we must have a low pass filter with high attenuation for frequencies higher or equal than $f_s=1/T$. Therefore the circuits will look like that one in figure 3 where the switch was replaced by a MOSFET controlled by PWM waveform.

$$\begin{aligned} v_o(t) &= V_i d + \sum_1^n a_n \cos 2n\pi f_s t + \sum_1^n b_n \cos 2n\pi f_s t \\ a_n &= \frac{V_i}{\pi n} \sin 2\pi n d \ldots\ldots\ldots\ldots b_n = \frac{V_i}{\pi n}(1-\cos 2\pi n d) \end{aligned} \tag{4}$$

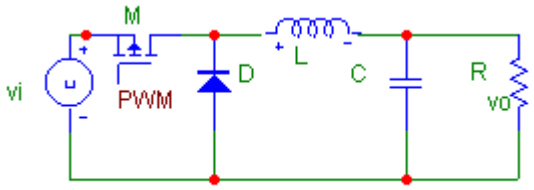

FIGURE 3 – Buck converter.

The function of diode D in the circuit above is to provide a path for the current during the time the switch is opened. At this moment the energy stored in the inductor's associated magnetic field needs to be released. So when s1 is opened the polarity of L is the opposite of that in figure 3 and de diode D is forward-biased providing a path for the current. We note that current is always flowing trough inductor L.

2 - Filter Design

Let's find the linear constant-coefficient second order differential equation that describes the filter in the circuit of figure 4.

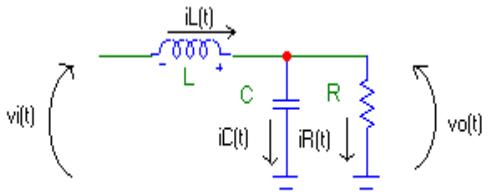

FIGURE 4- Filter circuit.

$$v_o(t) = Ri_R(t) \tag{5}$$

$$v_i(t) - v_o(t) = L\frac{di_L(t)}{dt} \tag{6}$$

$$i_C(t) = C\frac{dv_o(t)}{dt} \tag{7}$$

Combining (5),(6) and (7) leads to the following differential equation:

$$\frac{d^2y}{dt^2} + \frac{1}{RC}\frac{dy}{dt} + \frac{1}{LC}y = \frac{1}{LC}u \tag{8}$$

where $y=y(t)=v_o(t)$ and $u=u(t)=v_i(t)$

Applying Laplace transform to equation (8) we come up with the corresponding transfer function of the filter, assuming the initial conditions are zero.

$$\frac{Y(s)}{U(s)} = \frac{\frac{1}{LC}}{s^2 + \frac{s}{RC} + \frac{1}{LC}} \tag{9}$$

Equation (9) resembles the typical polynomial form of transfer function from differential equation as shown in equation (10)

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{10}$$

where the parameter ζ is the **damping ratio** and ω_n is the **undamped natural frequency**.
In communications and filter engineering, the standard second-order transfer function is written like in equation (11) where ω_0 is the **pole frequency** and Q is called the **pole quality factor**.

$$H(s) = \frac{\omega_0^2}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2} \tag{11}$$

$$p_1, p_2 = -\frac{\omega_0}{2Q} \pm j\omega_0\sqrt{1 - (1/4Q^2)} \tag{12}$$

The parameter Q determines the distance of the poles to the jω axis; the higher the values of Q, the closer the poles are to the jω axis and the more selective the filter response becomes, that is the selective factor becomes closer to unit and the filter gets closer to ideal. An infinite value of Q locates the pole on the jω axis and can yield to sustained oscillations and negative values of Q implies that the poles are in the right half of the s-plane, which certainly produces oscillations.

2.1 – Components evaluation

The next step is to size the inductor. To do this we need to look at the current waveform over the inductor.

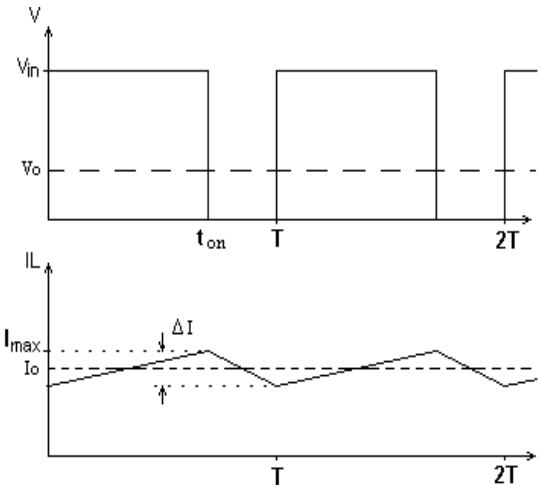

FIGURE 5 – Steady-State Waveform over the inductor.

The current across the inductor during the first interval when the switch is closed is given by

$$i(t) = \frac{1}{L}\int_{-\infty}^{t_{on}} v(t)dt \tag{13}$$

Therefore, during this time the voltage applied to the inductor is (V_{in}-V_o). The integral (13) can be solved evaluating the area of the rectangle delimited by V_{in} and t_{on}. The result is

$$\Delta I = \frac{1}{L}(v_{in} - v_o)t_{on} \tag{14}$$

Similarly

$$\Delta I = \frac{1}{L}v_o t_{off} \tag{15}$$

$$t_{off} = \frac{1 - \frac{v_o}{v_i}}{f_s} \tag{16}$$

Designing the inductor can be done in two ways, so during the time the switch is opened the energy stored at the inductor can provide a continuous or a discontinuous current at the output resulting in two standard modes of operations called continuous and discontinuous modes. In this project we are dealing with continuous mode. Let's first choose the switching frequency. Selecting a high frequency will be advantageous in the point of view of cost and weight since we get a small inductor, but there is a limit where a certain value of f_s will make the resistive component of the capacitor, ESR, greater than its reactance or the capacitor can resonate and from this frequency its electrical behavior can be like an inductor which certainly represents a disadvantage. Another aspect to be considered is the DC and switching losses in the active components such as the transistor and diode. Therefore a comparison table would be a good idea in selecting the value for fs.

TABLE -1 - Switching losses comparison.

Freq.	**50khz**	**100Khz**	**200khz**
Power output(W)	50	50	50
Conduction Power loss(Pc)(W)	10.8	10.8	10.8
Switching losses(Ps)(W)	1.4	2.8	5.6
Power input(W)	62.2	63.6	66.4
Efficiency	80.3	78.6	75.3

The values above are approximations and calculated based on a MOSFET losses according to the following equations where P_s is the loss for each type of transition(t_{on} or t_{off}), that is, P_s is the sum of losses for turned on and turned off transition times.

$$P_S = \frac{V_{DS(\max)} I_{D(\max)}}{2} \tau_S f_S$$

$$P_C = I^2_{D(RMS)} R_{DS(on)}$$

The chosen frequency in this project will be 100khz. Once we determine this frequency we can use equations (15) and (16) to come up with a value for L, since we intend to have a continuous mode design at nominal output current.

Having the input voltage ranging from 20 to 40V we have

$$t_{off\,(min)} = 7.5us$$

$$t_{off\,(máx)} = 8.75us$$

Since the inductor must be able to store enough energy during the off time, we must deal with the highest value for t_{off}

Regarding the range of ΔI, let denote I_{o1} the minimum specified load current and I_{o2} the maximum specified load current. So if we make ΔI/2 greater than I_{o1}, the current at the inductor will become negative and this is called discontinued mode. Although it's safe to operate at discontinuous mode frequency will change and the response becomes poor. So we choose $\Delta I=2.I_{o1}$. But as I_{o1} gets smaller so does ΔI, which according to (15) will result in large value for L. In the same way as we increase ΔI, L decrease, but the high peak current represented by $I_{o1}+\Delta I/2$ will cause components saturation. Here we assume $\Delta I_{max}=0.5.I_{o2}$ as a design condition.

2.2 – Components selection

In our example I_{o1}=2A, I_{o2}=10A. Therefore ΔI=4A which is a feasible value since it's bellow the limit $\Delta I_{max}=0.5\ I_{omax}$=5A. From (15) we get the value of L

$$L = \frac{V_o t_{off}}{\Delta I} = 10.9uH$$

The capacitor must be sized in order to fit the requirements of maximum output ripple. Figure 6 shows the waveforms over the capacitor

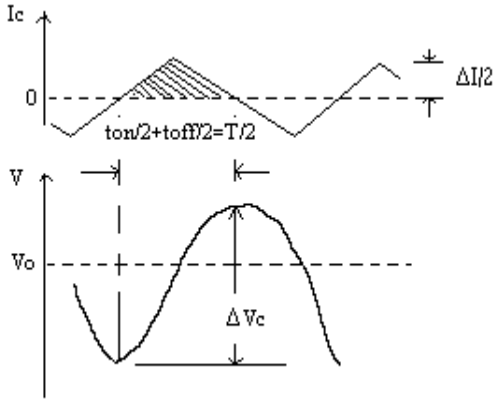

FIGURE 6-Capacitor waveforms.

ΔV_c is the ripple at the capacitor and can be calculated as

$$\Delta V_c = \frac{1}{C}\int i_c(t)dt$$

This integral can be evaluated by finding the area shown in the current waveform of figure 8.

$$\Delta V_c = \frac{\frac{\frac{T}{2}\frac{\Delta I}{2}}{2}}{C} = \frac{\Delta I}{8 f_s C} \tag{17}$$

$$C = \frac{\Delta I}{8 f_s \Delta V_c} = \frac{4}{8x100kx100x10^{-3}} = 50uF$$

3 – Simulation results

The values of components obtained so far are just a first approximation. Since the converter will work in a voltage loop we have to analyze the filter already designed inside the loop in order to assure loop stabilization Final adjustments might be necessary in order to achieve design specification. Having calculated the filter components let's now take a look at the open loop characteristic of the filter transfer function shown bellow for R=0.5Ω. Figure 7 shows the frequency response for the projected values using MATLAB.

$$G(s) = \frac{1.83 \times 10^{9}}{s^{2} + 40 \times 10^{3} s + 1.83 \times 10^{9}}$$

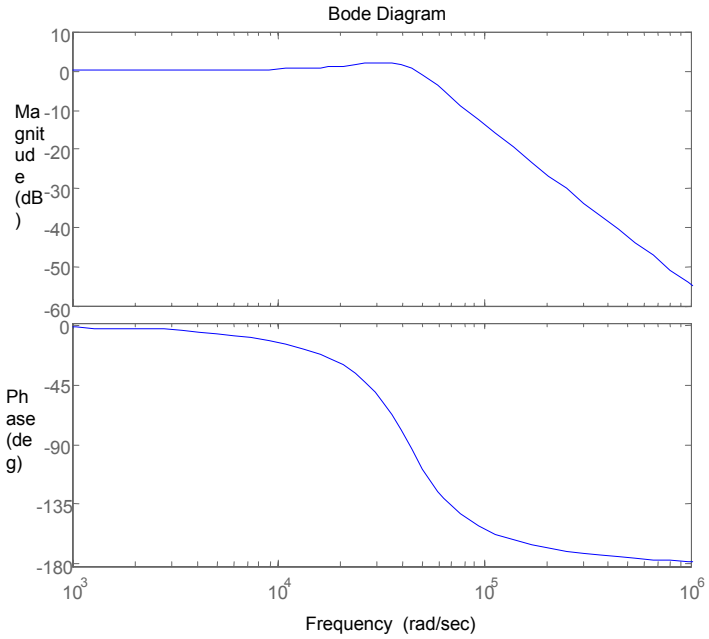

FIGURE 7-MATLAB simulation of filter frequency response.

We note that the filter by itself has a very low phase margin which needs to be increased. We will achieve a better phase margin by adding a suitable controller in a closed loop configuration.

4 - Compensation technique

Let's first take a look at a typical block diagram of our system, which is shown in figure 8 bellow. In this figure G(s) is the filter transfer function, V_i is the input voltage, 1/Vp represents the modulation of duty cycle according to the signal error *c* provided by the compensator C(s).

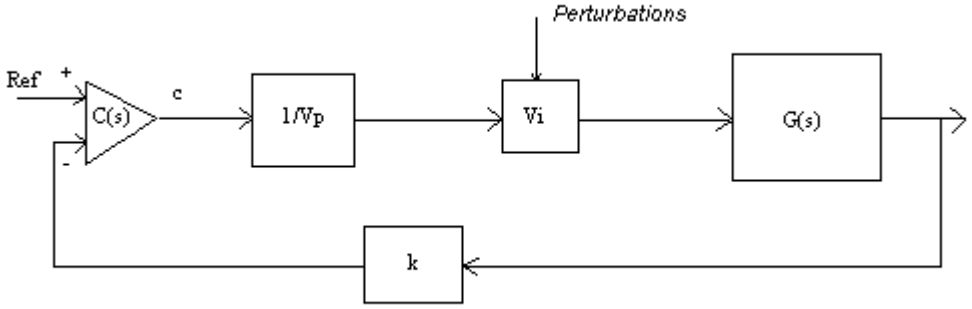

FIGURE 8 – System block diagram.

The open loop gain, according to control system definitions, is

$$G(s)H(s) = \frac{k\dfrac{V_i}{V_p}\dfrac{C(s)}{LC}}{s^2 + \dfrac{s}{RC} + \dfrac{1}{LC}} \tag{18}$$

H(s) in this case is a constant k which is a voltage divider of the output. For this example k=1/2. $1/V_p$ represents the typical modulator block where V_p=2.4 and V_i=40v. Because we want to see the system characteristics without compensation at this time just to get an idea about phase margin let's set C(s)=1 with no contribution in gain and phase. Substituting the values gives

$$G(s)H(s) = \frac{15.3\times10^9}{s^2 + 4\times10^4 s + 1.8\times10^9} \tag{19}$$

The Bode plot for equation (19) will look similar to that of figure 7 except for the gain factor. But the overall loop gain that it's desirable for this system is shown in the next figure. This is the gain after accounting the effect of the controller on the system.

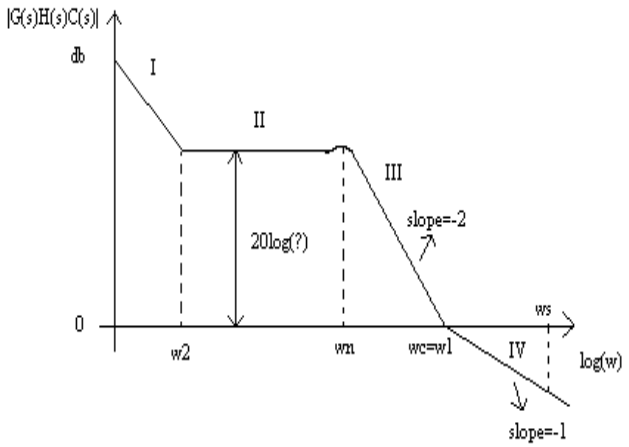

FIGURE 9 – Overall open loop gain.

Here are some considerations. We shape the gain to have an attenuation of –20db or more at the switching frequency w_s. This avoid large signals instability and attenuate the voltage ripple at the output. We place a zero at the cross over frequency w_c, which changes the slope from –2 to –1, so we set w_c one decade bellow w_s. Therefore we have an attenuation of –20dB at w_s. Moreover we have pole at zero frequency to keep the gain high at DC level because this keeps the input error of the controller very small. The frequency w2 is chosen one decade bellow the natural frequency w_n. The controller topology that has the characteristics for shaping this system is

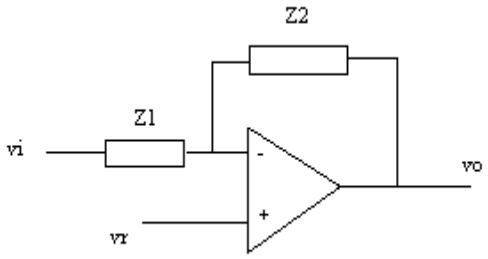

FIGURE 10 – Controller topology.

$$v_o = -\frac{Z2}{Z1}v_i + (1+\frac{Z2}{Z1})v_r = \frac{Z2}{Z1}(v_r - v_i) + v_r$$

$$C(s) = \frac{Z2}{Z1}$$

Let's choose convenient Z2 and Z1

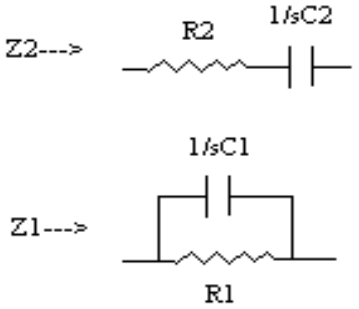

FIGURE 11 – Impedances.

$$Z2 = R2 + 1/sC2 = (R2C2s + 1)/sC2$$

$$Z1 = R1.1/sC1/(R1 + 1/sC1)$$

$$Z1 = (R1/sC1)/((R1C1s + 1)/sC1)$$

$$Z1 = R1/(R1C1s + 1)$$

$$C(s) = -\frac{Vo(s)}{Vi(s)} = \frac{Z2}{Z1} = \frac{(R1C1s + 1)(R2C2s + 1)}{R1C2s}$$

The bode sketch for this compensator is shown in the next figure. It's a lead-lag type compensator that subtracts phase at lower frequencies and adds phase at higher frequencies with no contribution in phase in the mid range.

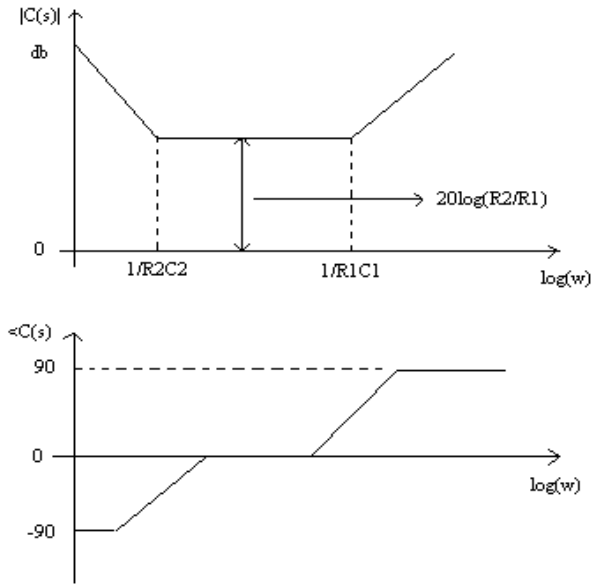

FIGURE 12 – Compensator's bode sketch.

4.1 – Compensator's component selection

Now we are ready to find out the components values.

Step1:

$$w_s = 2\pi f_s$$

$$w_c = 0.1 w_s$$

$$fs=100khz$$

$$ws=6.28x10^{5}rad/sec$$

$$wc=6.28x10^{4}rad/sec$$

Step2:

$$\mathbf{w_c=1/R1C1}$$

$$R1C1=1.59x10^{-5}$$

Step3:

Looking at figure 9 the expression 20log(?) is the sum of 20log(kVi/Vp) and 20log(R2/R1). So the gain at region II at figure 9 is 20log(kViR2/R1Vp).

We want the gain at w=w_c equal to zero. If the gain in db of |G(s)H(s)| at w_c is G1 then the controller shall have a gain of –G1. Therefore 20log(R2/R1)=-G1

$$\mathbf{R2/R1=10^{-G1/20}}$$

$$G1=13.4db$$

$$R2/R1=0.21$$

$$R1=10k\Omega$$

$$R2=2.1k\Omega$$

$$C1=1.6nF$$

Step 3:

$$\mathbf{W_2=0.1x1/(LC)^{1/2}}$$

$$W_2=4.28x10^{3}rad/sec$$

Step 4:

W_2=1/R2C2

$$R2C2=2.33x10^{-4}$$

$$C2=110.7nF$$

Now the design is completed. The transfer function along with the bode plot giving the overall gain and margin is shown

$$G(s)H(s)C(s)=\frac{1.53x10^{10}(3.7x10^{-9}s^2+2.5x10^{-4}s+1)}{1.11x10^{-4}s(s^2+4x10^4s+1.8x10^9)}$$

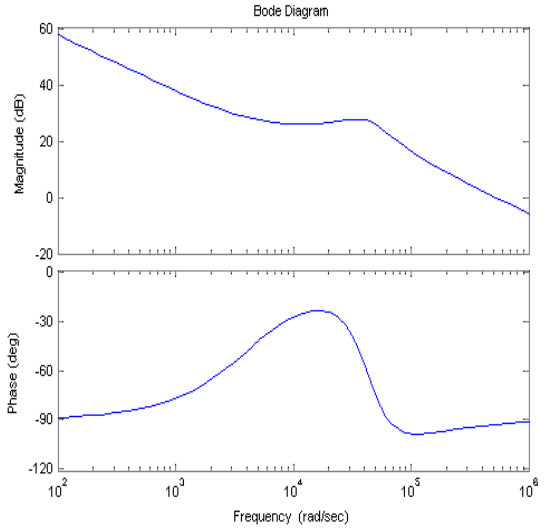

FIGURE 13 – Overall open loop gain.

5 – Lab results

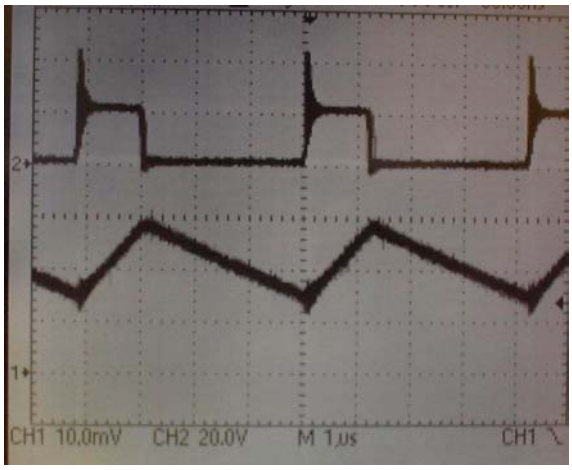

FIGURE 14 – Filter input voltage and inductor current.

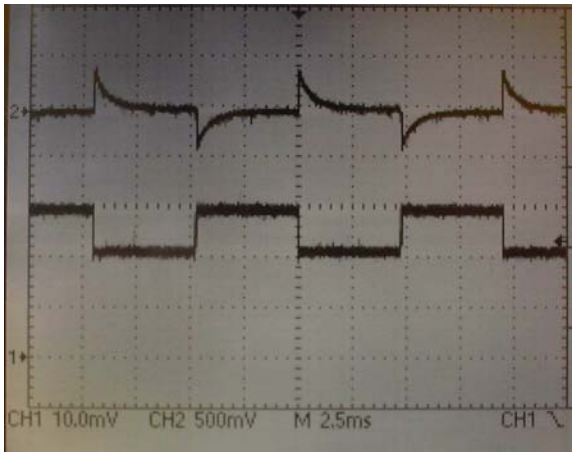

FIGURE 15 – Load transient.

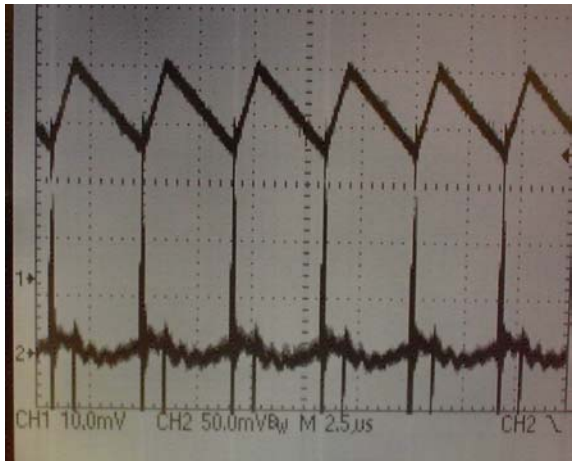

FIGURE 16 – Output ripple.

In the figure 14, the upper curve is the voltage input and the lower one is the inductor current. In the figure 15 the upper curve is the a-c variations of output voltage due to load transients represented by the lower curve. In the figure 16 the upper curve is the inductor current and the lower curve is the output voltage ripple.

All the results above were obtained after connecting a MOSFET as a load at the output and modulating its gate voltage with a square wave in order to have load transients as shown in figure 15. To measure the current we have used a current probe amplifier with scale of 1A/div. Note that the switching frequency has doubled from its original projected value. This is due to the type of driver used in the project, which will not be discussed here. One could decrease the oscillator frequency by half but we left it as built. Some remarks about this change are made at the conclusion section.

6 – Conclusion

We showed in this report that designing stable control loops for buck topology in voltage mode control is easily achieved by implementing the compensator described in previous section. Besides, some specifications were able to be verified after building a prototype which showed an efficiency in the order of 78%. Also within specification was the output ripple of 25mV peak-to-peak as shown in figure 16 on channel 2. This ripple is smaller than the original projected value due to the increase in frequency. Also, the inductor's ripple decreased by half for the same reason. From figure 15 we evaluate the output impedance as 400mV/1A as well as a response time to variations in the load of about 2ms.

7 – References

Chryssis, G. **High-frequency switching power supplies**. New York : McGraw-Hill, 1984. 221 p.

Mitchell, D; Mammano, B. Designing Stable Control Loops. In: Unitrode Texas instruments. **Power Supply Desgn Seminar.** Topic 5, p. 5-1 - 5-30, 2001 series

Unitrode. **International semiconductor databook**. Application Notes. 1982-1983

Sedra; S**. Microelectronic circuits**. 3 ed. Oxford: Oxford Press 1991. 1054 p.

Unitrode Integreted Circuit. Application notes. **Linear integrated circuits data and applications handbook**. Merrimach: Unitrode, p. 9-1 a 9-305, 1990.